**HO CHI MINH UNIVERSITY OF TECHNOLOGY**

**OFFICE FOR INTERNATIONAL STUDY PROGRAMS - OISP**

**Logic Design with HDL**

EXPERIMENT

**Introduction & Structural Model**

**Group information:**

| Class : Logic Design with HDL (Lab)  Group : 2 | Lecturer’s comment |
| --- | --- |
| Full name:   1. Nguyễn Văn Bình : 2153223 2. Lê Minh Quý : 2153758 3. Trần Hải Đăng : 2153297 4. Phạm Đức Trung : 2153928 |  |

**1 Introduction**

**1.1 Aims**

• Get familiar with Vivado software and the FPGA development flow.

• Get familiar with FPGA Arty-Z7 board.

• Practice in designing simple digital logic circuits with Verilog.

• Understand the hierarchical design principle.

• Practice in writing test benches for a designed module.

**1.2 Preparation**

• Read the laboratory materials before class.

• Revise chapter 0-3 about Verilog basic.

• Each group prepare at least one laptop with Vivado software installed.

**1.3 Documents and lab materials**

• M. Morris Mano, Michael D. Ciletti, Digital System with an Introduction to the Verilog HDL, VHDL,

and SystemVerilog, Pearson Education, Inc, 2017

• Lecture slides

• Arty-Z7-20-Master.xdc: Arty-Z7 constraint file.

• Guide for Installing Vivado.pdf : Guide for installing Vivado and getting started with Vivado and

Arty-Z7.

• dec1to2.v, mux2to1.v : 2-to-1 multiplexer module and its sub-module.

• mux2to2 tb.v: test bench to simulate the module mux2to1.

**1.4 Procedure**

For each exercise (also for further labs):

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• Read the requirements, then determine the input/output signals of your circuits.

• Make design idea of the circuit then using Verilog to model the circuit.

• Analysis & Synthesis the circuit with Vivado software.

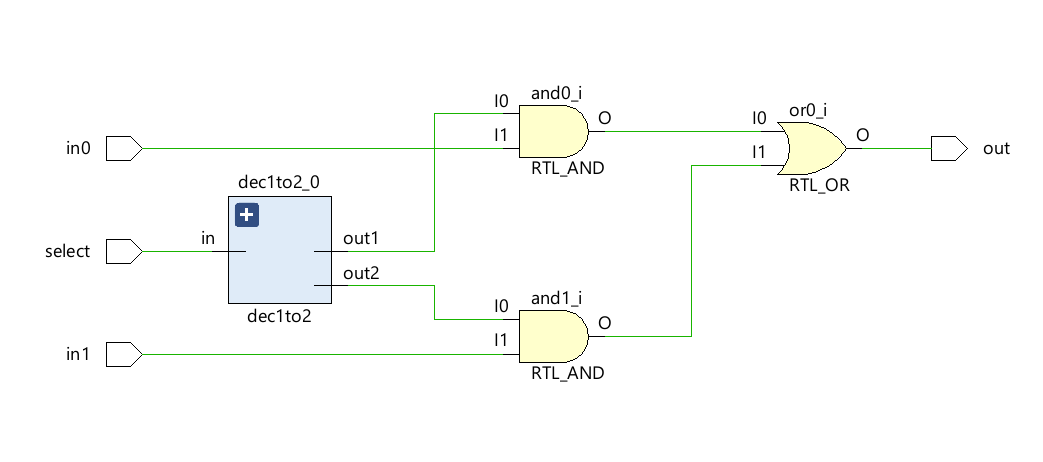
• Write test bench to simulate the circuit on Vivado Simulator.

• Generate the bitstream and program the Arty-Z7 to evaluate the circuit.

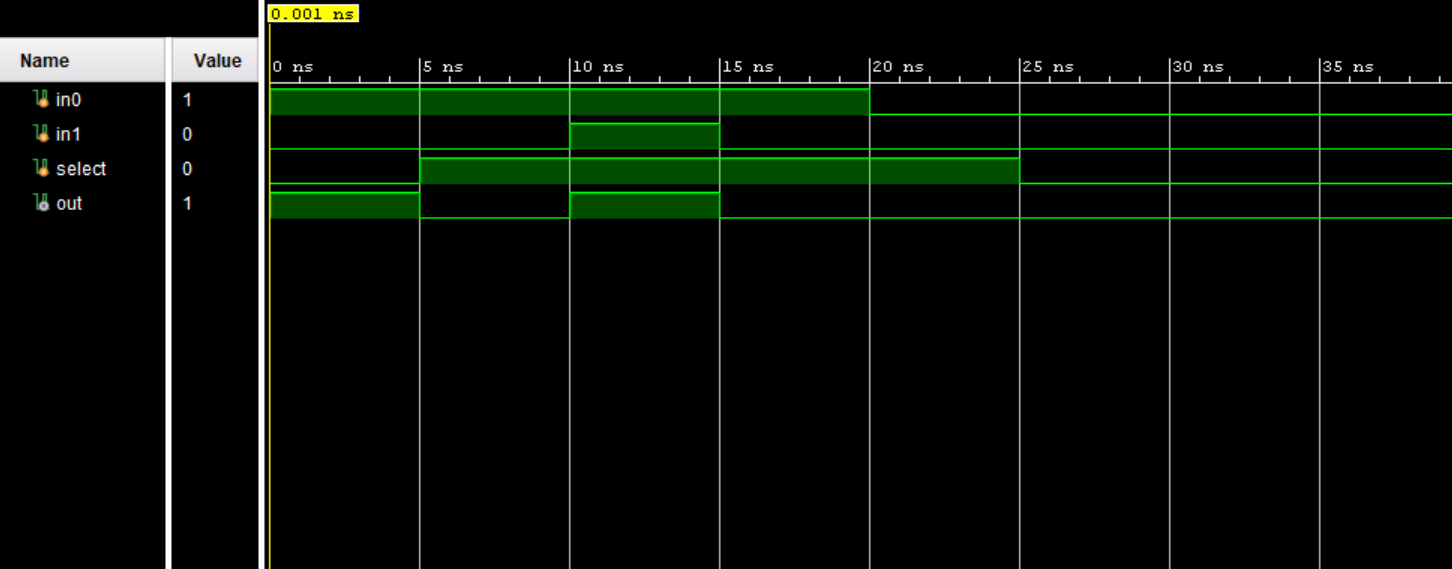
**2 Exercises**

**2.1 Excercises 1**

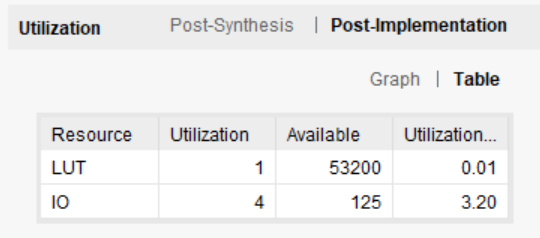
2.1.1 Name of source files

2.1.2 RTL Schematic

2.1.3 Waveform



2.1.4 Resource Utilization



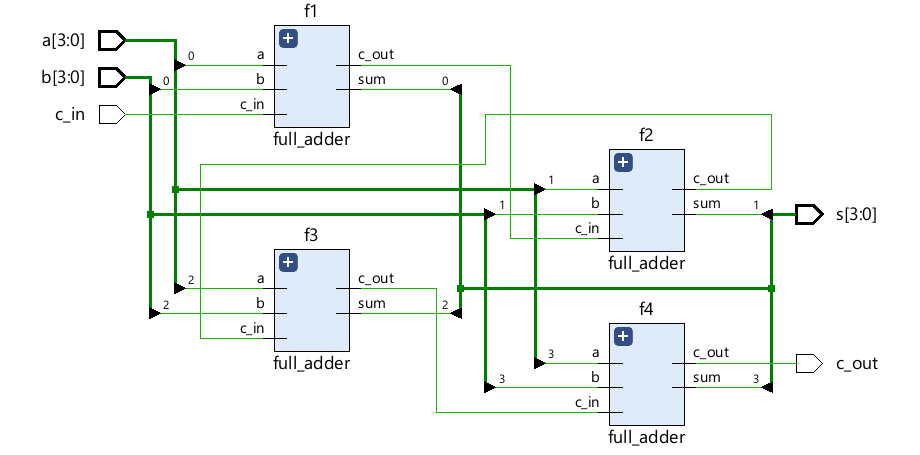
**2.2 Excercises 2**

**2.3 Excercises 3**

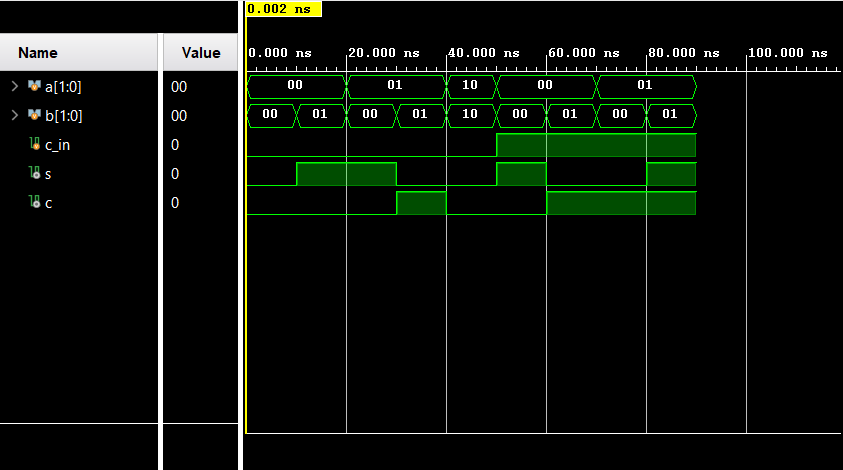
2.3 a,b.

- Name of source files : half\_adder.v, full\_adder.v

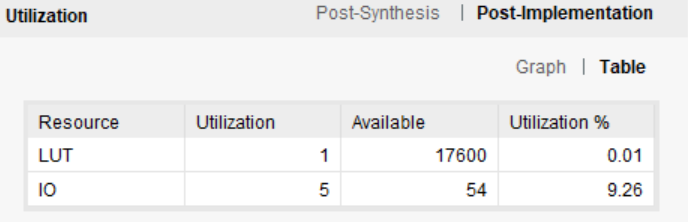
- RTL Schematic



- Waveform



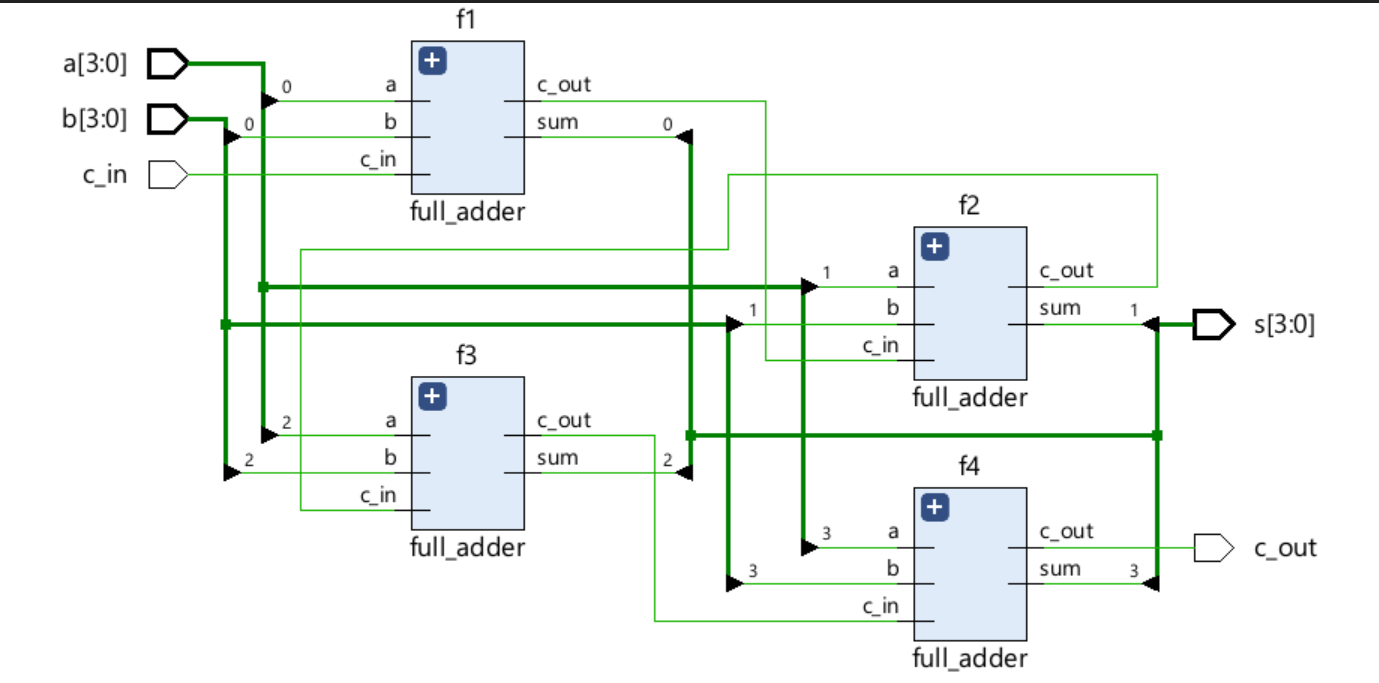
* Resource Utilization



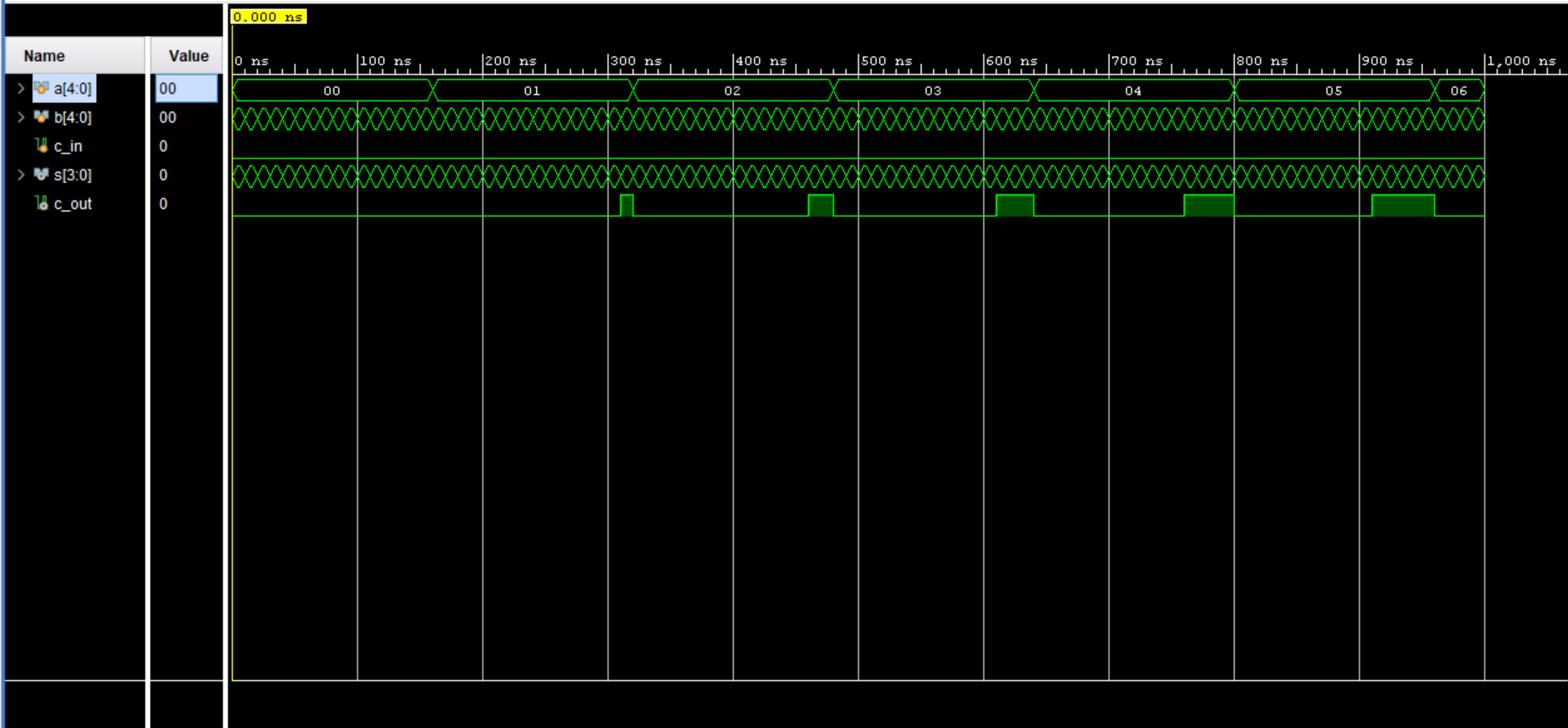
2.3 c

- Name of Source Files : adder4b.v, adder4b\_tb.v

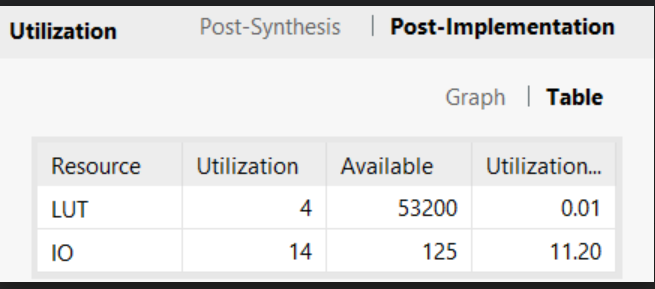
- RTL Schematic



- Waveform



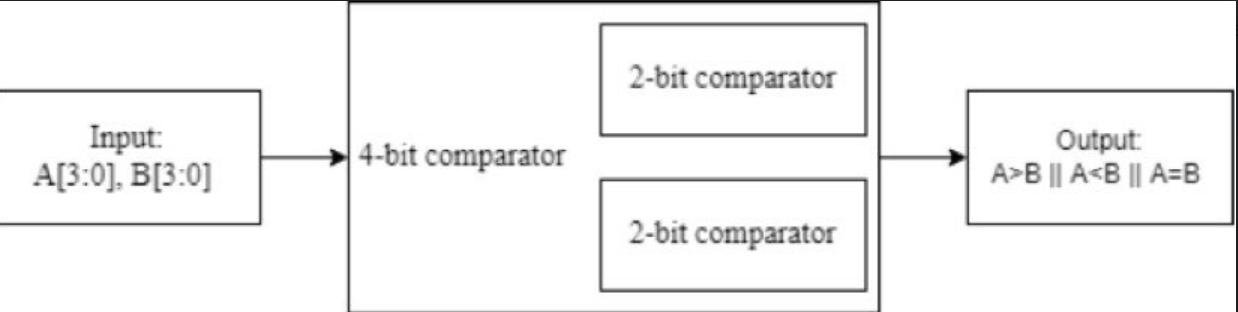
- Resource Utilization



**2.4 Excercises 4**

- Source files :

- A block diagram describes the idea:



- RTL Schematic

- Waveform

- Resource Utilization